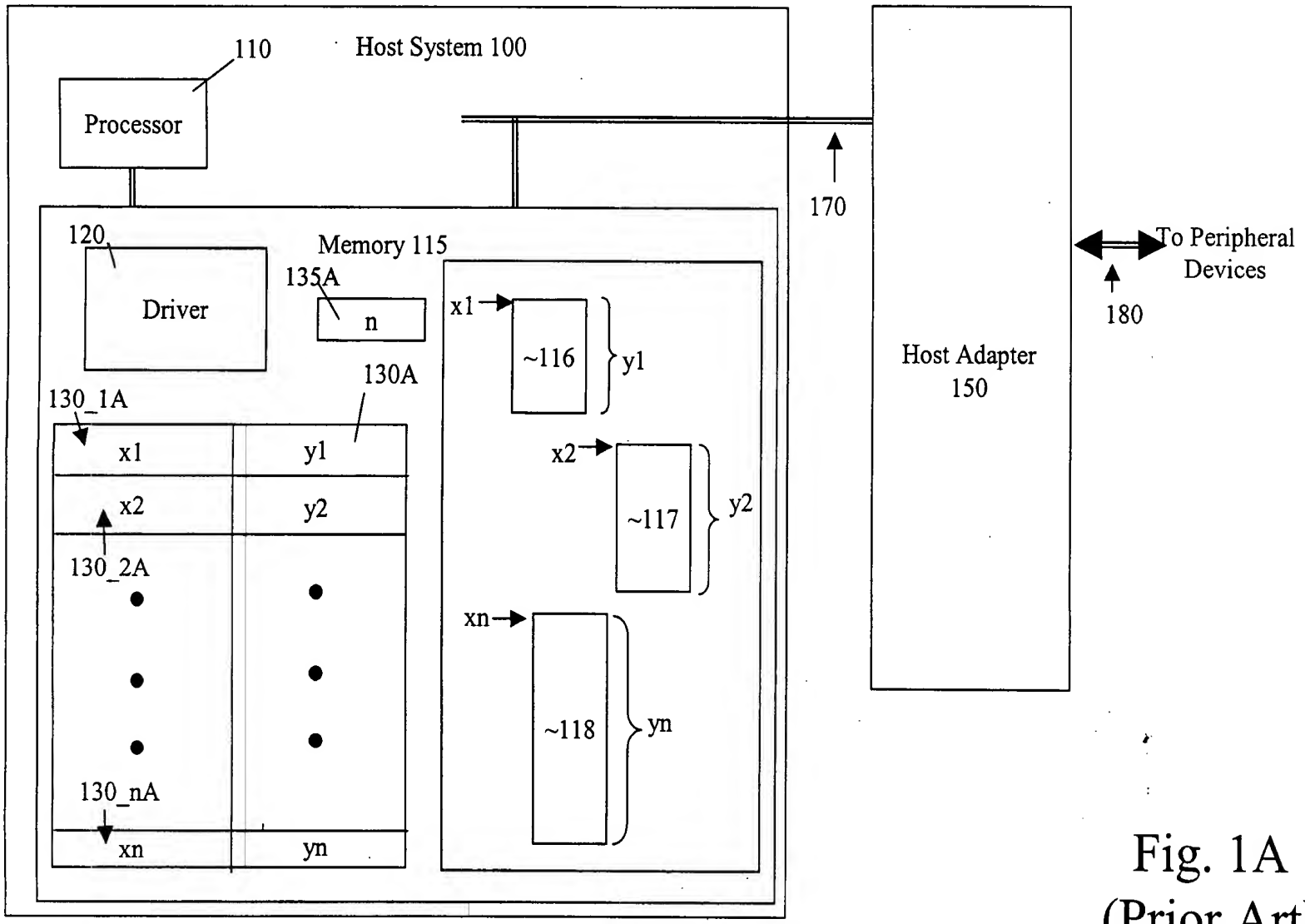


Fig. 1A
(Prior Art)

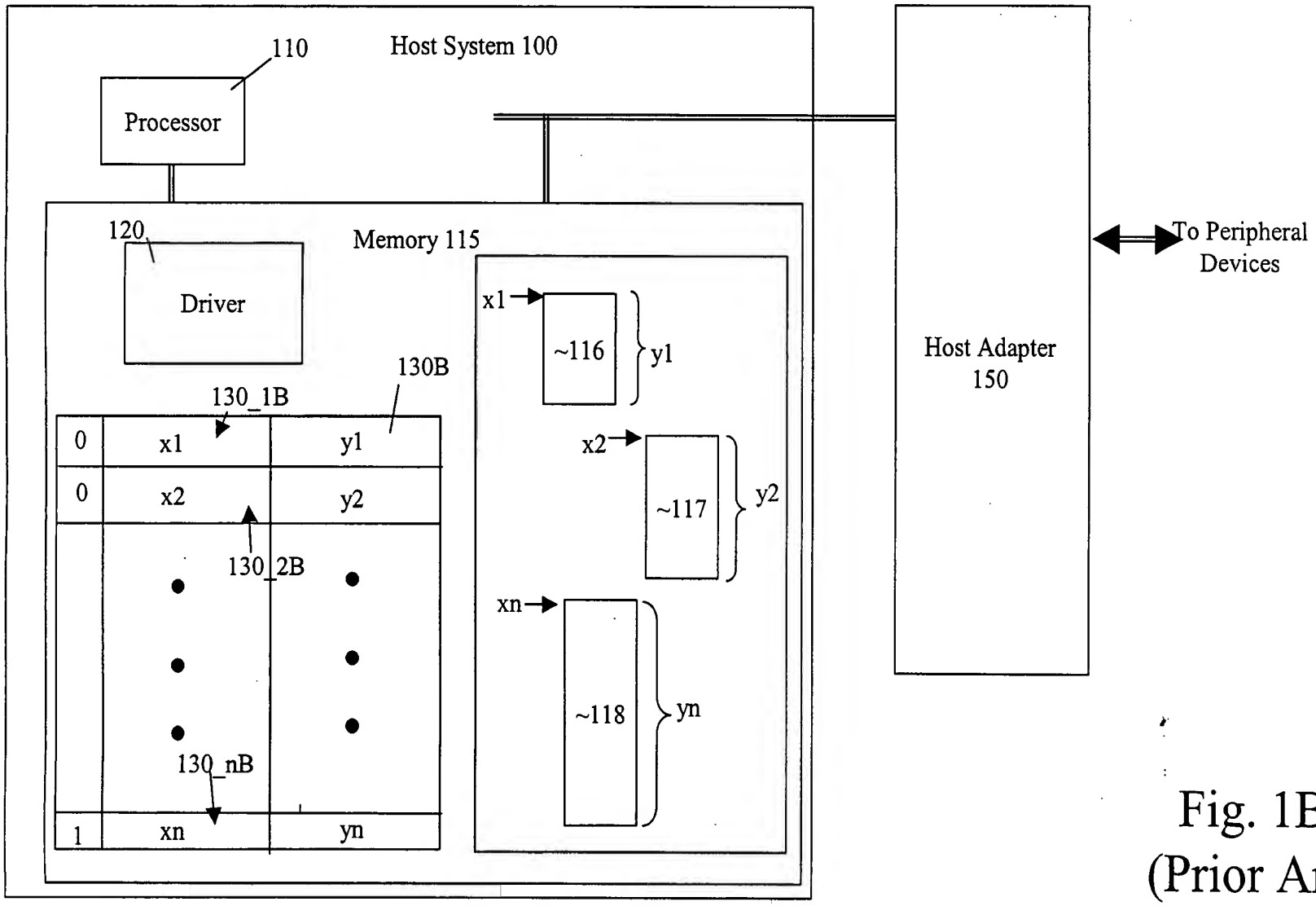


Fig. 1B
(Prior Art)

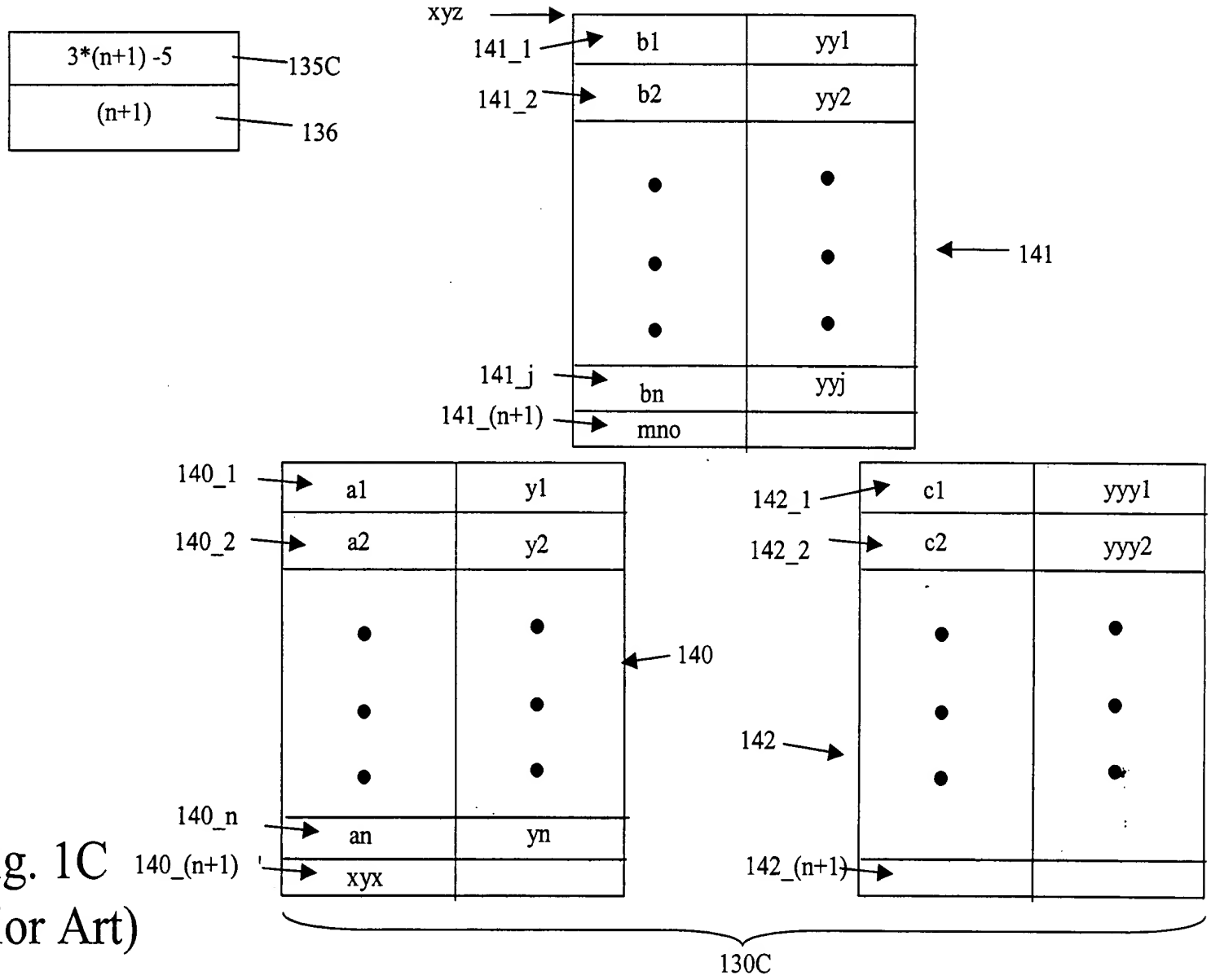


Fig. 1C
(Prior Art)

Fig. 2A

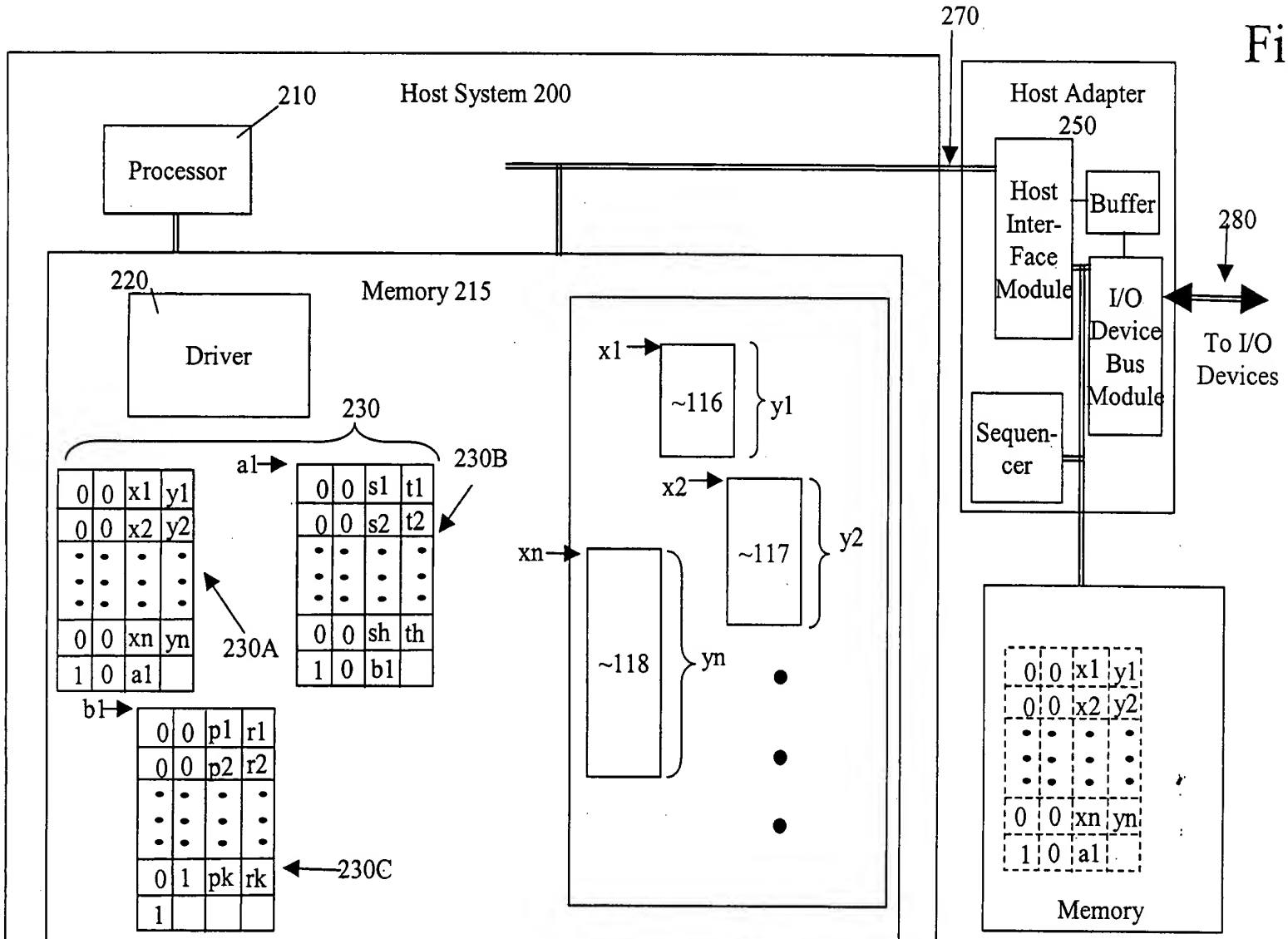

270
Host System 200
210
Processor
Host Adapter
250
Host Inter-Face Module
Buffer
280
I/O Device Bus Module
To I/O Devices
Sequen-cer
220
Driver
Memory 215
230
230B
a1
230A
b1
230C
x1
~116
y1
x2
~117
y2
xn
~118
yn
Memory

Fig. 2B

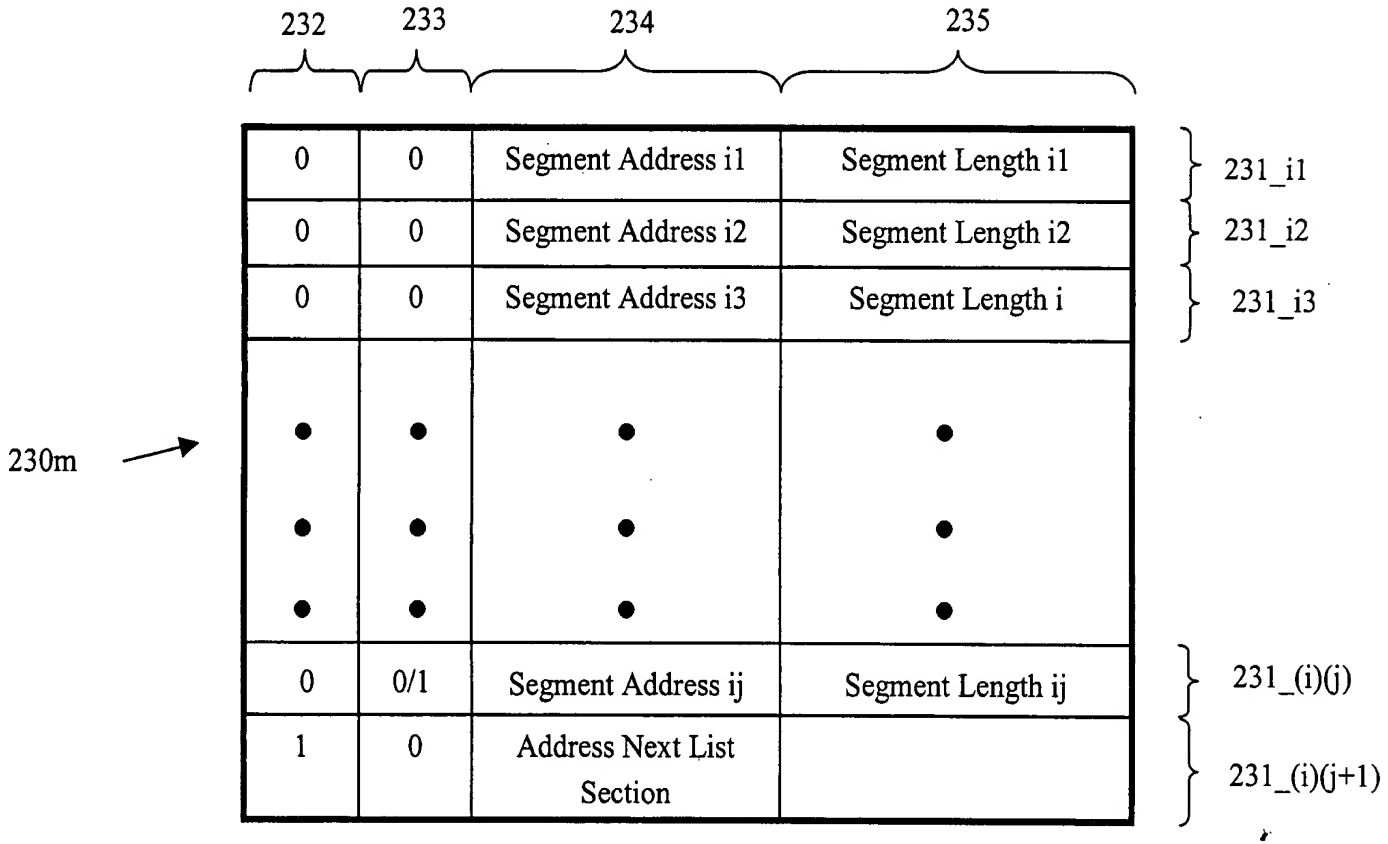

232
233
234
235
230m
0
0
Segment Address i1
Segment Length i1
231_i1
0
0
Segment Address i2
Segment Length i2
231_i2
0
0
Segment Address i3
Segment Length i
231_i3
0
0/1
Segment Address ij
Segment Length ij
231_(i)(j)
1
0
Address Next List Section
231_(i)(j+1)

Fig. 2C

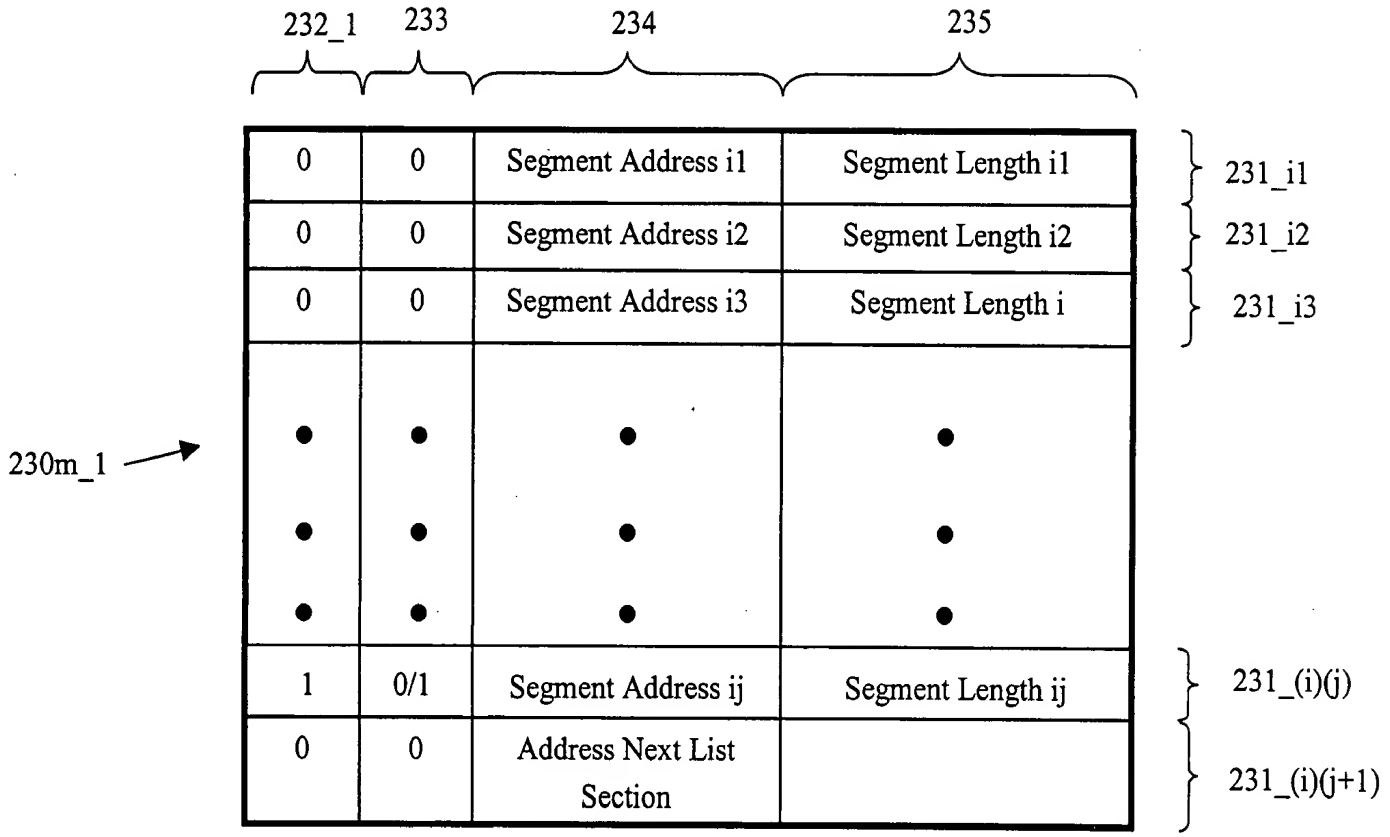

232_1
233
234
235
230m_1
0
0
Segment Address i1
Segment Length i1
231_i1
0
0
Segment Address i2
Segment Length i2
231_i2
0
0
Segment Address i3
Segment Length i
231_i3
1
0/1
Segment Address ij
Segment Length ij
231_(i)(j)
0
0
Address Next List Section
231_(i)(j+1)

Fig. 2D

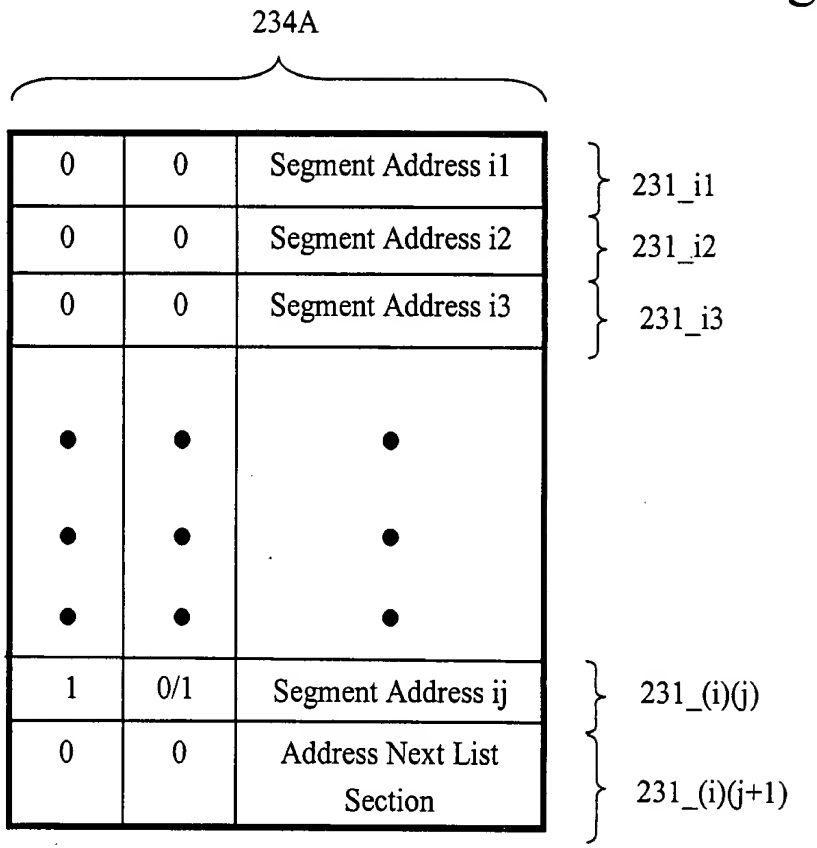
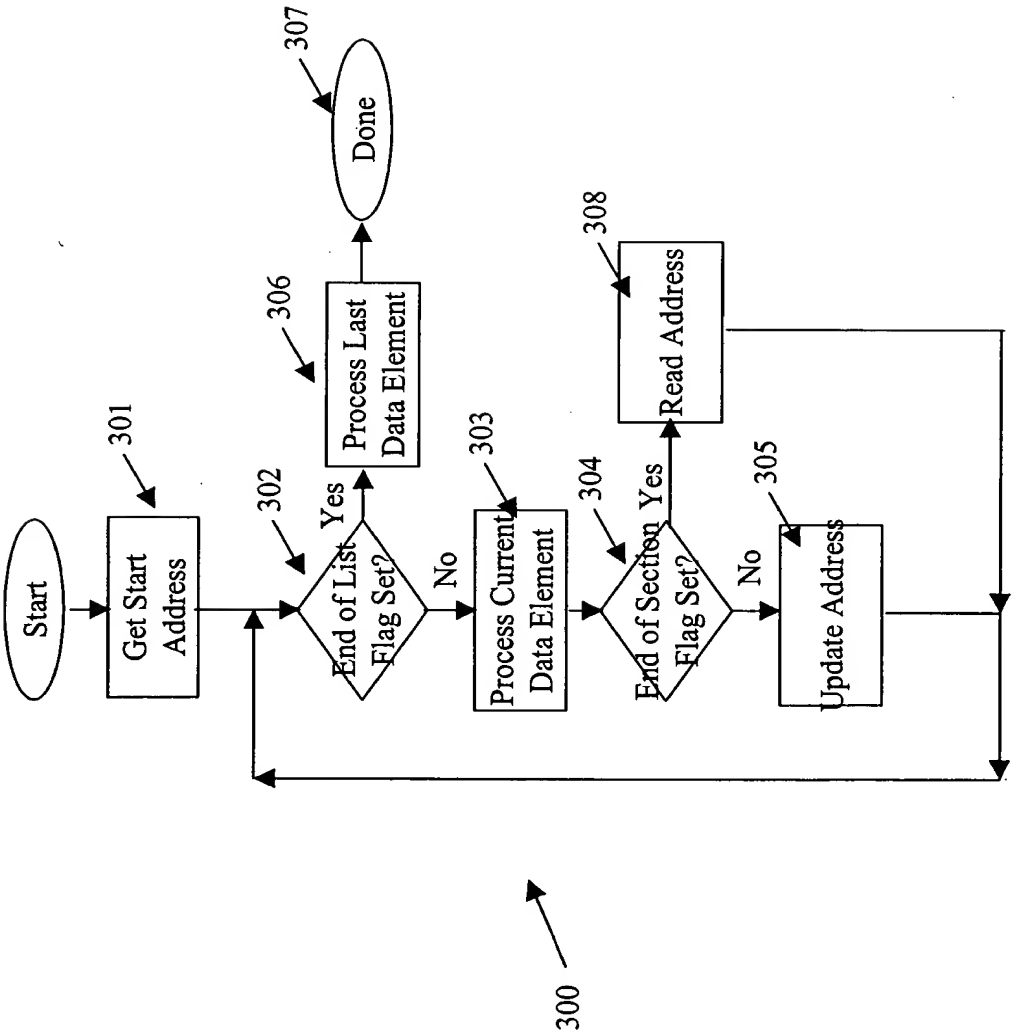

234A
0
0
Segment Address i1
231_i1
0
0
Segment Address i2
231_i2
0
0
Segment Address i3
231_i3
1
0/1
Segment Address ij
231_(i)(j)
0
0
Address Next List Section
231_(i)(j+1)

Fig. 3


Start
Get Start Address
301
End of List Flag Set?
302
Yes
No
Process Last Data Element
306
Done
307
Process Current Data Element
303
End of Section Flag Set?
304
Yes
No
Read Address
308
Update Address
305
300